UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/596,757	06/15/2000	Yibing Michelle Wang	08305/074001/99-15	3264

7590 02/10/2005

THOMAS J. D'AMICO
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
WILSON, JACQUELINE B	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/596,757	WANG ET AL.	
	Examiner	Art Unit	
	Jacqueline Wilson	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11 and 27-30* is/are allowed.

6)☒ Claim(s) *12,18,24-26,31 and 32* is/are rejected.

7)☒ Claim(s) *13-17, 19-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 08/31/04, with respect to the rejection(s)of claim(s) 1-32 under 35 USC § 102 and 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Park and Fossum et al.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US 5,714,753).

Regarding Claim 12, Park teaches imaging a scene by simultaneously obtaining both a high sensitivity signal (using a first photodiode 22) and a low sensitivity signal (using a second photodiode 24; see also the abstract) in each of a plurality of pixels (although Park teaches a light receiving portion, one having ordinary skill would recognize that a plurality of pixels are used in an imaging device and that only one is disclosed for simplicity). Park further teaches the high and low sensitivities are obtained within the pixel itself (referred to as light receiving portion), and outputting both of the

high and low sensitivity signal (via first and second transmitting gates (30a and 30b). However, Park does not specifically disclose low and high sensitivities using an integration period that is at least 80% overlapping for both high and low sensitivity. However, Park teaches that each photodiode has different potential well levels, one smaller than the other (col. 2, lines 45+). The examiner believes that depending on the manufacturer at the time the invention was made, it would have been an obvious matter of design choice to use low and high sensitivities using an integration period that is at least 80% overlapping for both high and low sensitivity for the purpose of having an image sensor with extended dynamic range and sensitivity. Since Parks teaches that the first photodiode 22 is larger than the second photodiode 24, it would have been obvious to use 80% overlapping for both high and low sensitivity to achieve the desired goal. Therefore, it would have been obvious to one having ordinary skill in the art to include low and high sensitivities using an integration period that is at least 80% overlapping for both high and low sensitivity for the purpose of having a extended dynamic range image sensor.

Claim 31 is analyzed and discussed with respect to Claim 12. (See rejection of Claim 12 above.)

Regarding Claim 32, Park fails to specifically teach storing the two different signals into respective sample and hold circuits. However, it is notoriously well known in the art to use S/H circuits for temporarily maintaining image signals for further processing. Typically, sample and hold circuits are used as a means for sampling and holding the signal charges in accordance with a timing signal (Official Notice).

4. Claims 18; and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al (US 6,665,013).

Regarding Claim 18, Fossum teaches a single continuous substrate of semiconductor material (see fig. 2; element 20), an image sensor portion formed on the substrate including an array of image sensor pixels arranged in rows and columns (20), including photoreceptors (fig. 3, element 30), each formed of a MOS electronic component (col. 4, lines 56+), an image processing portion (referred to as a readout circuit 70), also formed on the substrate (see fig. 3), and connected to said image sensor portion such that each pixel can be selectively coupled (via row select circuit 60) to a specified portion of the image processing portion (200 and 225), the image processing portion including a plurality of transistors (see fig. 3, 200 and 225 are among the plurality of transistors), each of which are formed of MOS transistors and a plurality of which are formed of MOS transistors (col. 4, lines 57+). Fossum further teaches a control portion which controls integration of the photoreceptors in the image sensor portion including times of integrations (referred to as integration periods; inherently taught in col. 3, lines 40-col. 4, lines 4), and also controlling connections between the image sensor and the image processing portion, (col. 3, lines 45+), and controlling timing operations in the image processing portion (also inherent since voltage values are used to operate the image processing portion (col. 4, lines 5-35). Fossum further teaches each of the pixels and the image sensor includes a photoreceptor (fig. 3, 30), a transfer gate (35), an associated portion (40) that selectively receives charge from the

photoreceptor via the transfer gate (col. 3, lines 60+), a reset transistor (referred to as a reset electrode 45), a follower transistor (referred to as source follower FET 55), coupled to the associated portion (see fig. 3), and operating to buffer the value of the associated portion, and a selection transistor (60) inherently coupled to the control portion, the control portion controlling the selection transistor to produce an output from the specified pixel (in a specified row) such that a level of the associated portion is first sensed (referred to as reset the charges in the floating diffusion 40), and then values are coupled from the photoreceptor into the floating diffusion and to sample values on the floating diffusion, the values provided to the image processing portion (col. 3, lines 40-55).

Regarding Claim 24, Fossum teaches the image processing portion includes a plurality of image processing circuits (220 and 245), arranged such that one image processing circuit is associated with an entire column of the image sensor pixels (referred to as column select FET), and the control circuit inherently controls the image sensor pixels to select an entire row of image sensor pixels at one time (via row select transistor 60), the entire selected row being coupled simultaneously to different ones of the image processing circuits to determine values therefrom to thereby operate to output an entire column in parallel (col. 4, lines 5-34; see fig. 3).

Regarding Claim 25, Fossum teaches a reset transistror in each of the pixels (although one pixel is shown, col. 3, lines 8-9, the circuitry is taught for all pixels in the array as shown in fig. 2).

Regarding Claim 26, Fossum teaches the control portion controls integration times of both the photogate and the floating diffusion by controlling the reset transistor to the floating diffusion to first reset the floating diffusion, then control the select transistor to sample the level on the floating diffusion (col. 3, lines 40-55).

Allowable Subject Matter

5. Claims 13-17, and 19-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 13, the prior art neither teaches nor fairly suggests imaging a scene by simultaneously obtaining both a high sensitivity signal and a low sensitivity signal in each of a plurality of pixels of an image sensing device, using an integration period which is at least 80% overlapping for both high sensitivity signal and a low sensitivity signal, both the high and low sensitivity signals being obtained within the pixel itself, and outputting both the high and low sensitivity signals, as claimed in Claim 12, wherein the obtaining comprises providing both a photosensor and an associated device that is associated with the photosensor which normally obtains charge from the photosensor, **the photosensor obtaining the high sensitivity signal and the associated device obtaining the low sensitivity signal**.

Regarding Claim 19, the prior art neither teaches nor fairly suggests a single continuous substrate of semiconductor material, an image sensor portion, an image processing portion, a control portion, wherein each of the pixels and the image sensor

including a photoreceptor, a transfer gate, and an associated portion that selectively received charge from the photoreceptor via the transfer gate, a reset transistor, a follower transistor, couple to the associated portion, and operating to buffer the value of the associated portion , and a selection transistor, coupled to the control portion, the control portion controlling the selection transistor to produce an output from the specified pixel such that a level of the associated portion is first sensed, then values are coupled from the photoreceptor into the floating diffusion and to sample values on the floating diffusion and to sample values on the floating diffusion, the values provided to the image processing portion, as claimed in claim 18, wherein the image processing portion includes a plurality of sample and hold circuits therein, including a reset sample and hold which samples a reset level, **associated device sample and hold circuit which samples the level of the associated device**, and a photoreceptor sample and hold which samples a level of the photoreceptor.

6. Claims 1-11, and 27-30 are allowed.

Regarding Claim 1, the prior art neither teaches nor fairly suggests an image sensor comprising, a plurality of image sensing pixel portions; and plurality of image processing portions; each said image sensing pixel portion including a photoreceptor, which has a first sensitivity to light and produces charge based on an amount of incident light, and associated portion for said photoreceptor, **which associated portion selectively receives charge from said photoreceptor but which by itself has a second sensitivity to light different than said first sensitivity to light and**

produces charge based on an amount of incident light, an in-pixel follower transistor, and an in-pixel select transistor; and **wherein each said image processing portion includes circuitry that produces an output indicative of both an amount of charge received by said associated portion, and amount of charge received by said photoreceptor,** as claimed in Claim 1.

Regarding Claim 27, the prior art neither teaches nor fairly suggests a method of obtaining images of different sensitivities, comprising: floating diffusion associated with a photogate; **first sampling a level of integration which has occurred in said floating diffusion** and **then transferring charge from said photogate to said floating diffusion and sampling the level that has occurred in said photogate**; outputting two values indicative respectively of **a low sensitivity signal and a high sensitivity signal that were integrated at substantially the same time, based on floating diffusion signal and said photogate signal**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacqueline Wilson whose telephone number is (703) 308-5080. The examiner can normally be reached on 8:30am-5:00pm (alternate Fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JW
02/01/05

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600